Early End of Life Failures of Electronics in Avionic Systems

Joseph B. Bernstein

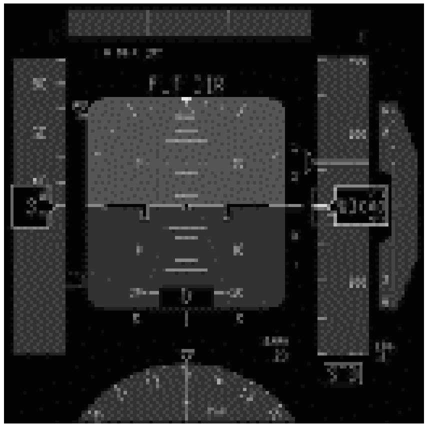
Associate Professor of Reliabilty

UNIVERSITY OF MARYLAND
1856

Sponsored by:

Aerospace Vehicle Systems Institute - AVSI

Texas Engineering Experiment Station
Texas A&M University



May 2001

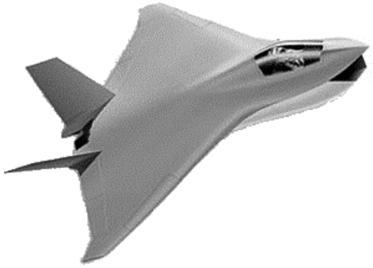
AVSI Project

- Sponsored by a consortium of Aerospace companies
  - Future avionics systems will be designed, built, operated and maintained using standard, commercially available, electronic components
  - The electronics industry trends are moving counter to aerospace industry needs
  - The aerospace industry can no longer assume that the life of a Line Replaceable Unit (LRU) will be greater then 5-10 years.

Methods to Account for Accelerated Semiconductor Device Wearout

AVSI Project #17

College Park, MD



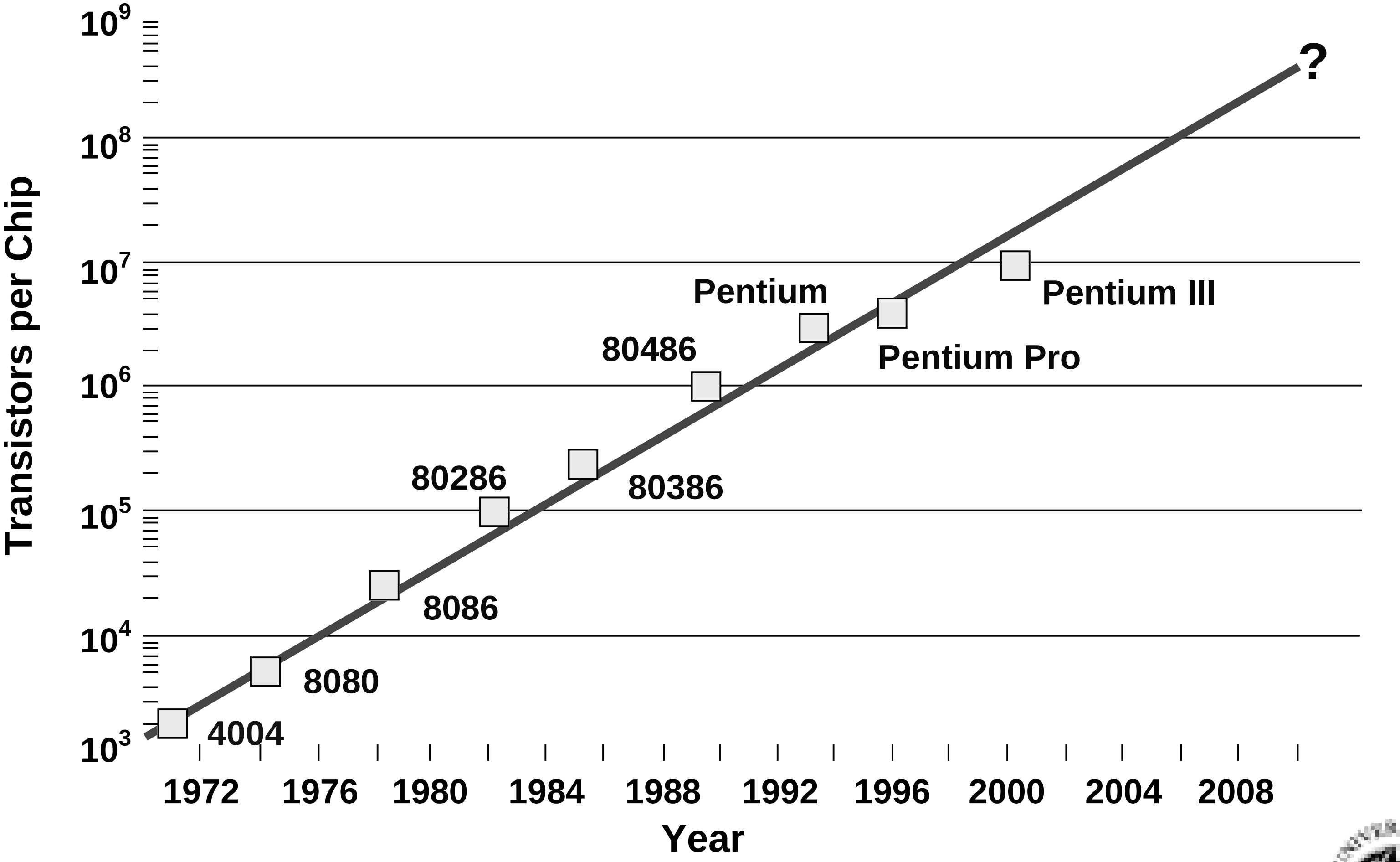
Lloyd Condra, PI
Boeing
425-266-5975

lloyd.w.condra@boeing.com

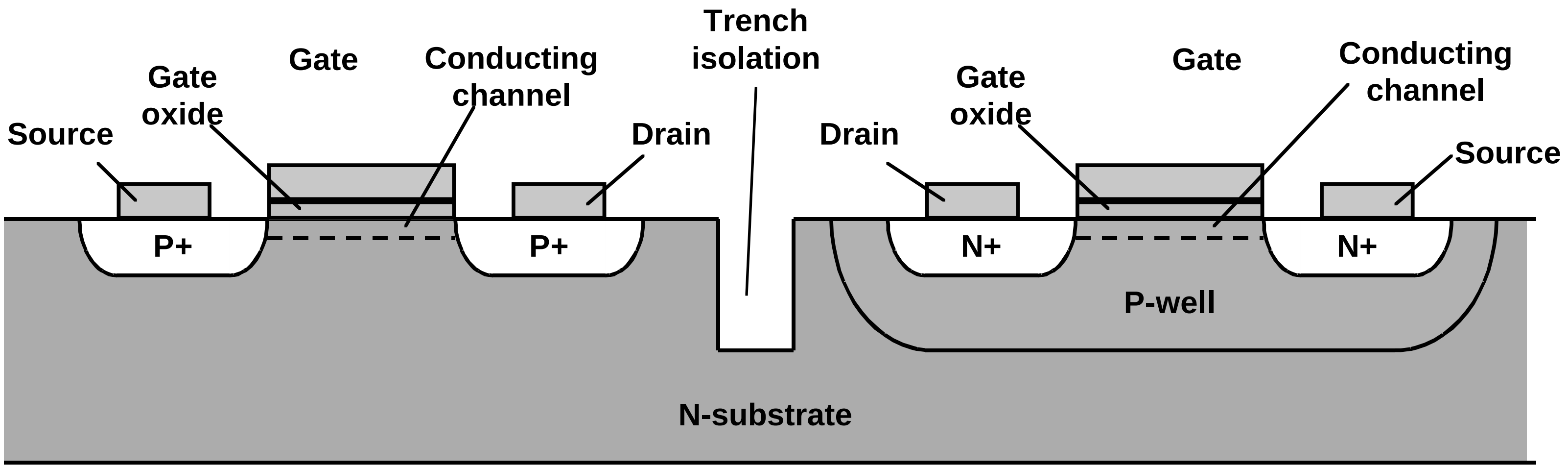
Assumptions

- Future avionics systems must be designed, produced, operated, maintained, and supported using commercially-available electronic components
- The electronic component industry is moving counter to aerospace interests
- We cannot assume that the design, production, or service life of an individual LRU will be greater than 5-10 years

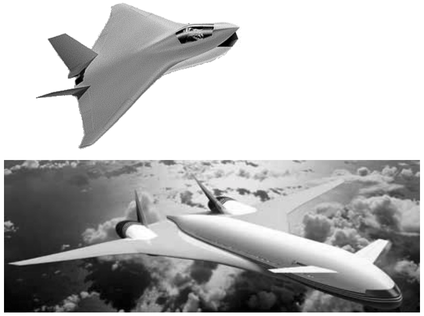
The Whole Problem: Moore's Law



CMOS Gates

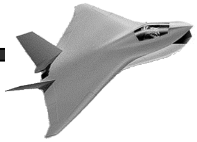

Trench isolation
Gate
Conducting channel
Gate oxide
Source
Drain
Drain
Gate oxide
Gate
Conducting channel
Source
P+
P+
N+
N+
P-well
N-substrate

Technical Trends



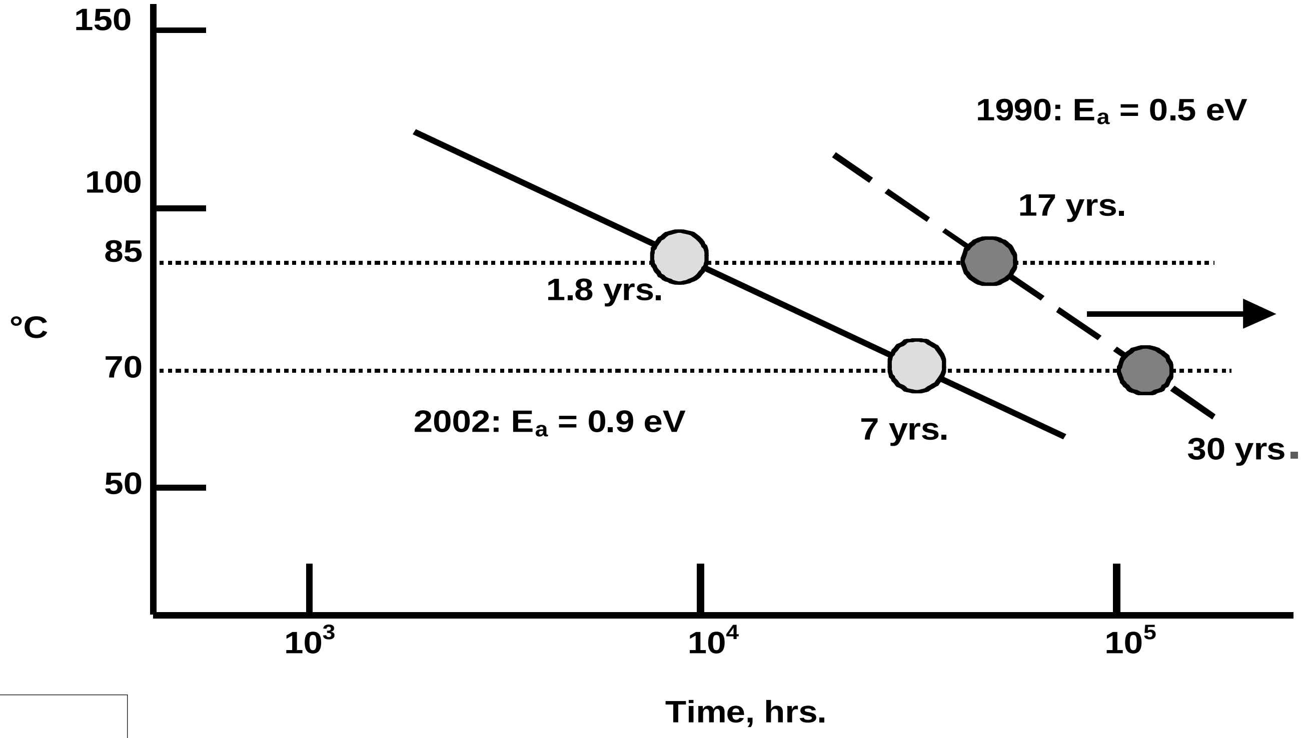
	1990	2002	**2005**	2014
Million transistors per chip	**1**	100	**190**	4,308
Local clock frequency, MHz	**33**	2,100	**3,500**	13,500
MPU Gate length, nm	**600**	90	**65**	22
Gate oxide thickness, nm	**12**	2.2	**1.3**	0.6

More Technical Trends



	1990	2000	2010
Operating temperature, °C	-55 to 125	-40 to +85	0 to 70
Supply voltage	5v	1.5v	0.6v
Max. power (high perf.)	5	100	170
No. of package types	<10	<60	??
Design support life	>10 yrs.	1-5 yrs.	<1yr.
Production life	>10 yrs.	3-5 yrs.	<3yrs.
Service life	***>20 yrs.***	***5-10 yrs.***	***<5yrs.***

Device Wearout Trend



- **Estimated lifetimes at case temperatures of 70ºC (typical of desktops) and 85ºC (typical of avionics) for semiconductor devices produced in 1990 and 2002.**

Semiconductor Device Wearout

- Device manufacturers face relentless pressure to improve functionality and reduce costs
- Their major customers are willing to accept shorter device lifetimes in order get lower prices and improved functionality
- Aerospace customers must use the same products as the major device customers

Device Wearout Life

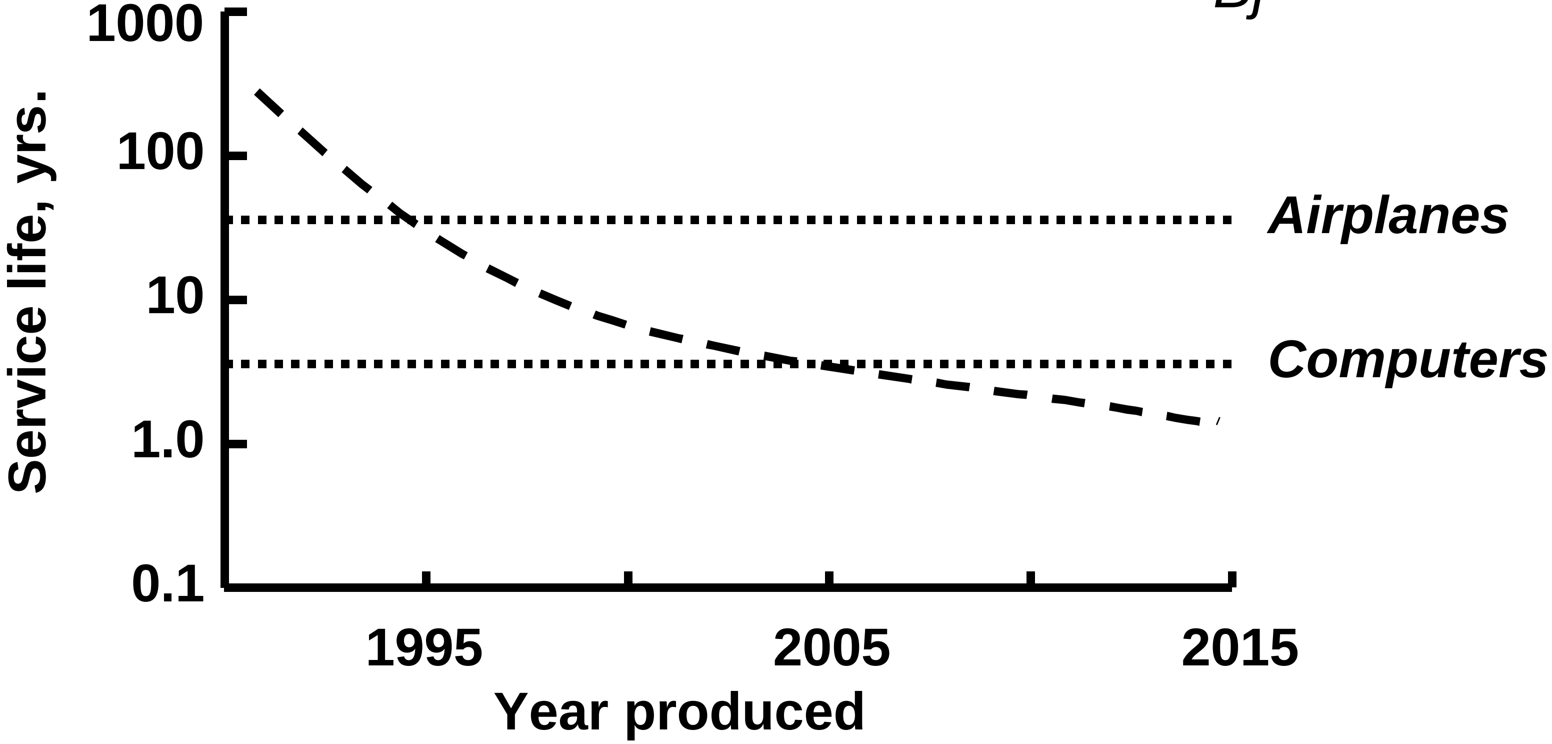
- **LSI Logic**
  - Current industry standard life tests are only equivalent to 10-year life
  - Rules can permit a customer to design for early wearout
- **TI**
  - FIT rates quoted are for 10-year life (80% of customers
  - Do not want to design for <10-year life, but will do so on request
- **Motorola**
  - Industry is reviewing 3 categories: 3-5 years, 5-7 years, 10+ years

Wearout Mechanisms

- *Package defects:* Understood, technical issues can be managed for future parts.
- *Silicon defects:* Understood, fundamental limitation on chip yield and extrinsic defects.
- *Electromigration:* Understood, may be less problematic for multiple layers of metal.
- *Oxide breakdown:* Technical limitations with ***no known technical solutions***

Electromigration

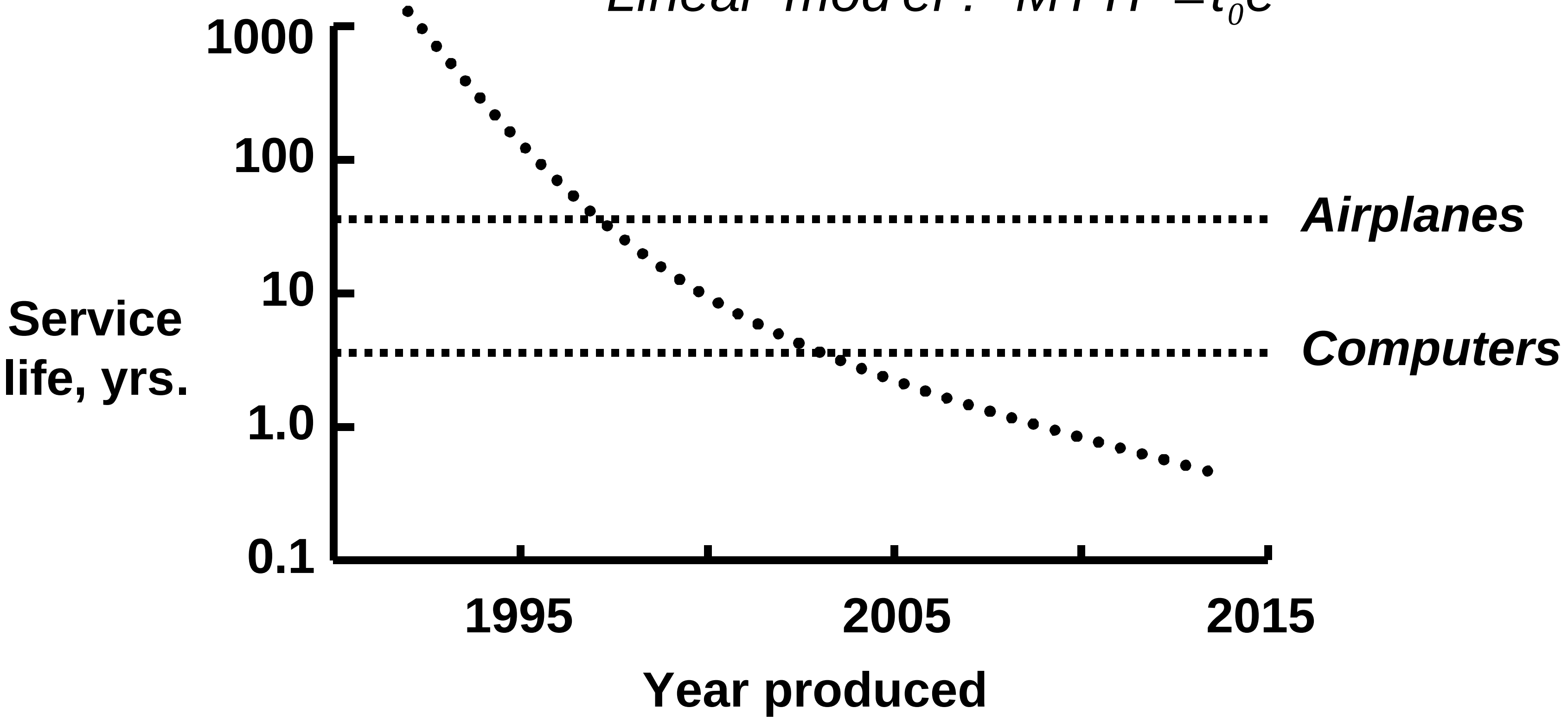
$$\text{Black's equation} : MTTF = \frac{wt}{Bj^{n}} e^{E_a / kT}$$



Mitigating factors: multilayer designs, Cu conductors, voltage scaling (probably will not be a show-stopper)

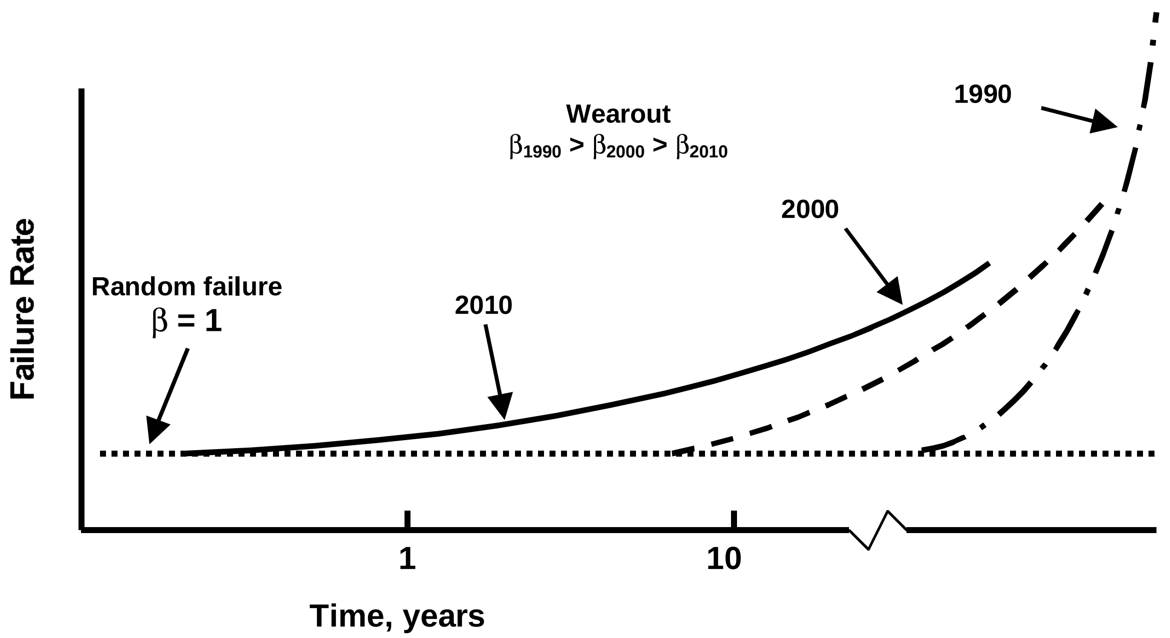
Oxide Breakdown

$$\text{Linear model: } MTTF = t_0 e^{(E-E_0)\gamma}$$



Mitigating factors: no known technical options

Reliability and Safety Assessment

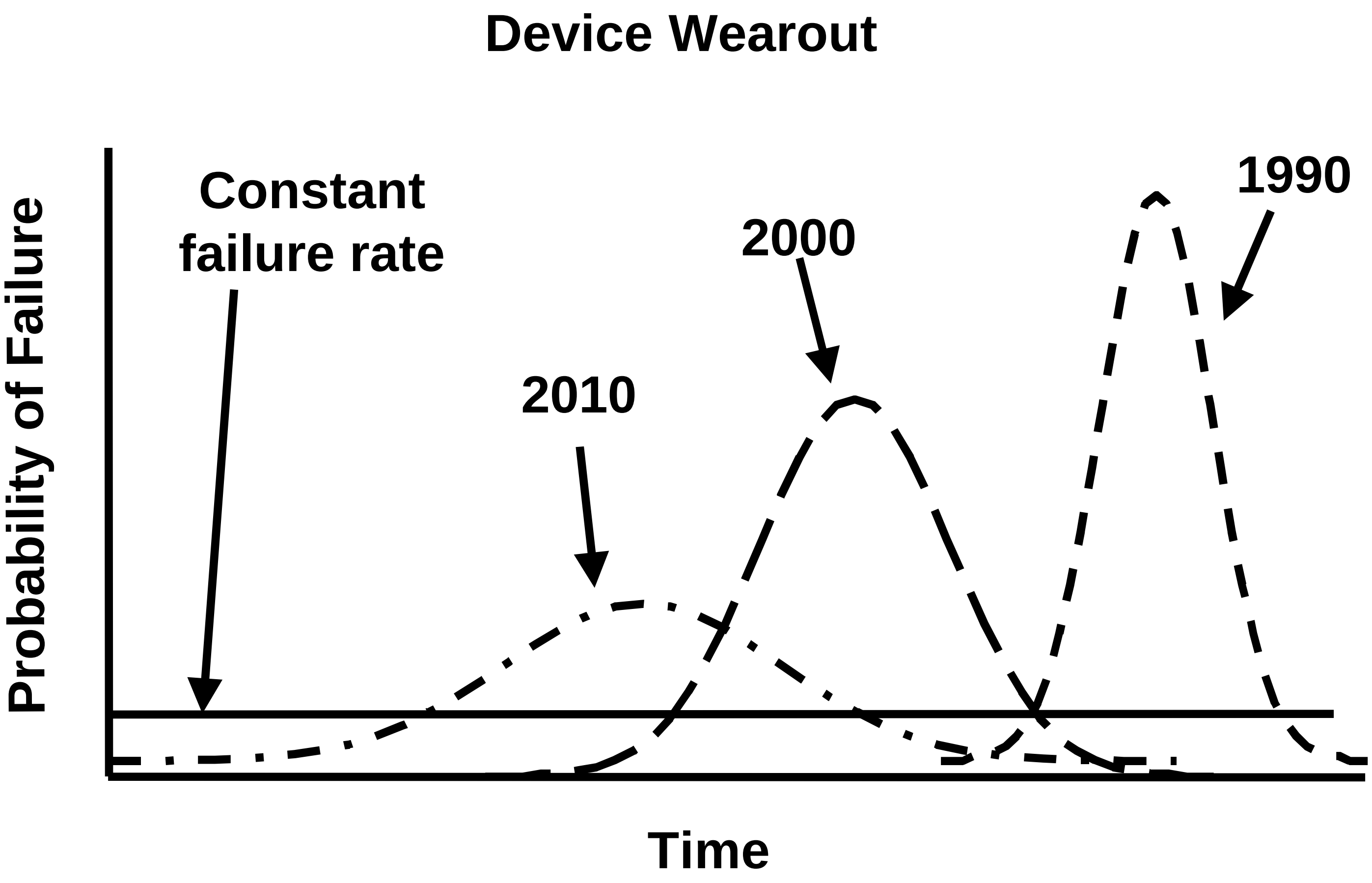


- Short device service life means that constant failure rate assumption (used in all current aerospace reliability and safety analyses) is no longer true
- Device failures may be considered common cause failures

Reliability Assessment

- **Determine failure distributions for semiconductor devices**
  - Will require accelerated testing of devices
  - Will require retrospectivly analyzing Field Failure data
  - Will be a continuing effort
- **Use Numerical Simulation Tools to estimate**
  - System failure rates
  - Time to system wearout (most important)
- **Reliability assessment will be an ongoing activity for each system**.

Effects of Early Wearout



What Will it Cost?

- Assume
  - A commercial jetliner has 300 electronics boxes
  - Each box costs $20,000
  - Each box will have to be replaced every 6 years
  - Replacement equipment cost is the same as original equipment cost
- Result
  - The added support cost will be $1M per airplane per year

AVSI Project Goals

- Conduct a Reliability Assessment of Semiconductor Devices
    - Determine failure distributions for semiconductor devices
    - Understand the effects of early wearout
    - Develop safety and reliability tools, process and guidelines for avionics system design
    - Estimate the Cost Impact on Future Generation Avionic Electronic Systems

UMD Project Organization

- We'll organize the project into 3 phases
  - Phase I will examine what is known today about avionics and component reliability
  - Phase II will examine component reliability in greater depth and develop screening approaches
  - Phase III will focus on understanding/predicting reliability and developing tools and process to design reliability into avionics systems
- The organization is a "living document" and will evolve

Project Organization

- Phase 1: Current Knowledge
  - Compile models on wear-out mechanisms including electromigration, hot-carrier degradation and oxide breakdown
    - Summarize results of literature search in a paper
    - Plan to submit paper to IEEE Transactions on Reliability.
      - *No proprietary* data will be in the paper.
    - Deliverable: Likely failure mechanisms of future semiconductor devices in avionics applications

Project Organization

- Get field data from AVSI members
  - Interested in building a baseline understanding of current avionics reliability and reliability processes
  - Not a critique of current processes
- Work with a “burn-in” house such as Bell Technologies and Amkor
  - Get test and field data on components
    - Get data on large numbers of a single component
    - Correlate Burn-In data with Field Failure data
    - Develop Screening tools for Reliability (I.e. Chip-Eye Technology methodology)

Project Organization

- Phase II: Understanding Failure Mechanisms
  - Complete analysis of field and burn-in data
    - Correlate models with field and test data
  - Deliverable: Develop Models to Estimate Lifetimes of Future Avionics
    - Verify Models
    - Continue Field Data analysis

Project Organization

- Phase III: Design Tools
  - Develop methodologies and tools to aid in the design of reliable avionics systems
    - Component lifetime modeling and selection
    - System level design techniques
  - Deliverables
    - Device Assessment Methods and Avionics System Design Guidelines
    - Adequacy of Existing System Reliability and Safety Analysis Methods for Future Avionics Systems

What we need from AVSI members

- LRU (Blackbox) Level
  - Failure rate
    - Number of failures
    - Operating time
    - Question: Is the operating time for avionics boxes measured in flight hours or actual powered-on time?
  - Operating conditions/environment
  - Failure modes/mechanisms

What we need from AVSI members

- Component Level
  - Component Failure Rates
  - Component environment
  - Failure modes/mechanisms
- Current processes for:
  - Reliability at the system level
  - Reliability at the component level
    - Component selection
    - Component qualification
  - Regulatory Guidance/Requirements
- We'd like to get as much raw field data as possible on failures

Areas of Wearout Concern

- Areas of wearout concern at the IC level
  - Electromigration
  - Oxide Breakdown
  - Hot Carriers
  - Packaging and Connections

Electromigration

- The movement of conductor atoms due to the flow of electrons
- Understood phenomenon
  - Can be dealt with through
    - The proper use of materials
      - Addition of Cu to Al interconnects
    - Multiple layers of metallization to reduce current densities
- Life time grows as linewidths shrink to 2μm
  - Due to grain structure assuming a ‘bamboo’ pattern

Hot Carrier Injection (HCI)

- Degradation of gate oxide performance
  - Typically results in reduced circuit speed (rather than hard failure)
- Effects are strongly influenced by voltage
  - **Decreased** temperatures INCREASES effects
- Don’t know if HCI will be a reliability concern
  - Evidence that the physics change at 0.25 μm and smaller
  - Some avionics systems spend time at LOW temperatures and some at HIGH temperatures.

Time Dependant Dielectric Breakdown (TDDB)—Oxide Breakdown

- Application of electric field across a dielectric material causes breakdown eventually resulting a short circuit failure
- Three step process
  - Defect generation during electrical stress
  - Breakdown trigger
  - Dielectric Breakdown
- This is expected to be an area of concern as device features shrink
  - No known technical solutions

Time Dependant Dielectric Breakdown

- Thermo-Chemical or E-Model
  - Field driven model
  - Trap generation begins with oxygen vacancy

$$t_{50} = e^{E_a / kT}$$

- Anode Hole Injection (AHI) or I/E-Model
  - Function of stress current density
  - Trapping of holes generated in Oxides

$$t_{BD} \cup e^{(B+H)/E}$$

Direction

- Bring together published literature and student research
  - Determine the significance and impact of the different wearout mechanisms
  - Understand and predict the lifetimes of semiconductor devices
  - Develop guidelines for designers of semiconductor devices
  - Develop guidelines for developer of higher level systems
  - Evaluate Economic Impact of Reliability